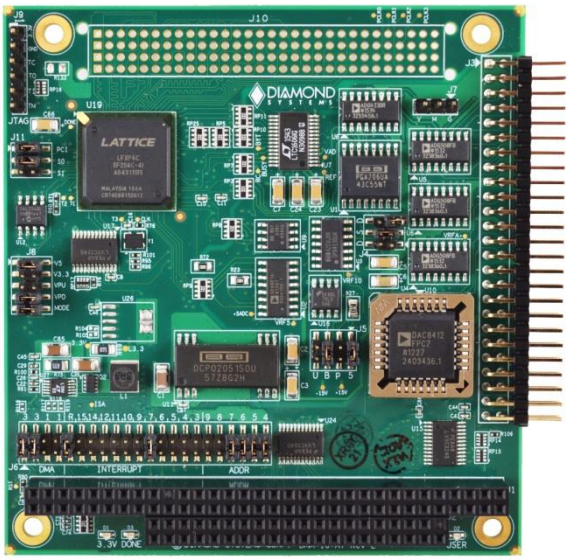
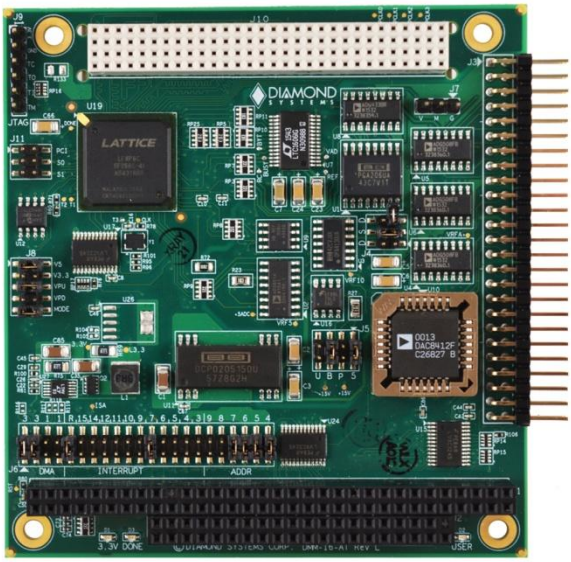
DMM-16R-AT / DMM-16RP-AT

Autocalibrating 16-bit Analog I/O PC/104 and PC/104-Plus Modules

User Manual V1.31



DMM-16R-AT



DMM-16RP-AT

Revision	Date	Comment
1.29	02/10/2017	Initial Release
1.30	02/13/2017	Updates throughout manual
1.31	9/12/2017	Update on accessing DIO ports

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1. DESCRIPTION

Diamond-MM-16R-AT (DMM-16R-AT) is a PC/104 (ISA bus) expansion board offering embedded systems designers a full feature set of data acquisition capabilities. It is designed to be used in any PC-compatible embedded computer with a PC/104 ISA bus expansion connector. DMM-16RP-AT is the same board with the PCI-104 connector installed to support both PCI and ISA bus interface.

The board is an upgraded version of Diamond Systems' DMM-16-AT board with backwards hardware and software compatibility to allow system upgrade without any redesign in most applications.

Upgraded features include:

- Direction control for both 8-bit digital I/O ports (DMM-16-AT has 1 fixed input and 1 fixed output port)
- 5V/3.3V level selection for digital I/Os
- Jumper selectable pull-up or pull-down option for digital I/Os
- User programmable blue LED
- PC/104-Plus PCI interface support (model DMM-16RP-AT only)

NOTE: For simplicity, in this manual the term "DMM-16R-AT" may be used to refer to both the PC/104 and the PC/104-Plus models of the board. In instances where the information is specific to one model, the text will say "DMM-16R-AT only" or "DMM-16RP-AT only" or other similar clarifying language.

Key features include:

Analog Input

- 16 single-ended / 8 differential inputs
- 16-bit A/D resolution
- 100KHz maximum aggregate A/D sampling rate
- Programmable input ranges with maximum range of +/-10V
- Both bipolar and unipolar input ranges
- 512-sample FIFO for reliable high-speed sampling
- Autocalibrated inputs

Analog Output

- 4 12-bit analog outputs
- Fixed and user-programmable output ranges
- Single-channel and simultaneous update
- Autocalibrated outputs

Digital I/O

- 16 digital I/Os 3.3V/5V TTL compatible
- Input/ Output direction control

Counter/Timers

- 1 32-bit counter/timer for A/D sampling rate control
- 1 16-bit counter/timer for user counting and timing functions
- Programmable clock source for user counter/timer

System Features

- +5V-only operation
- Extended temperature range (-40 to +85^{o}C)
- Connector pinout compatible with Diamond-MM-16-AT board
- Register map compatible with Diamond-MM-16-AT board

2. BLOCK DIAGRAMS

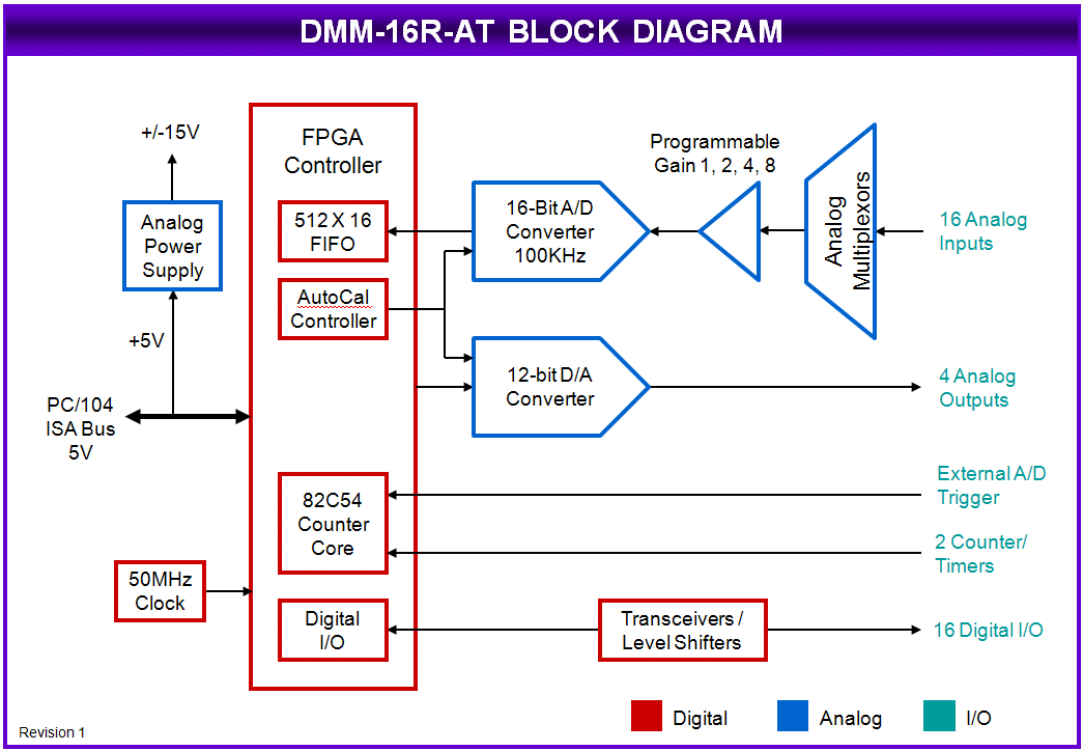


Figure 1 DMM-16R-AT Block Diagram

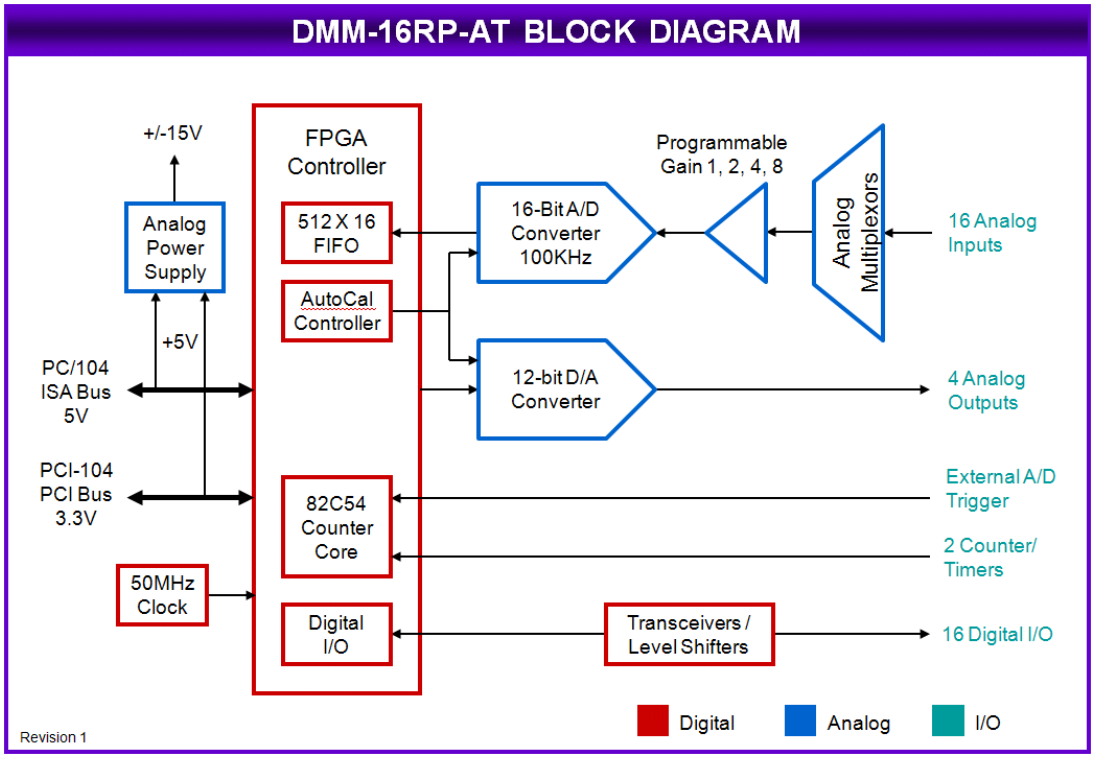


Figure 2 DMM-16RP-AT Block Diagram

3. MECHANICAL DRAWING AND FEATURES

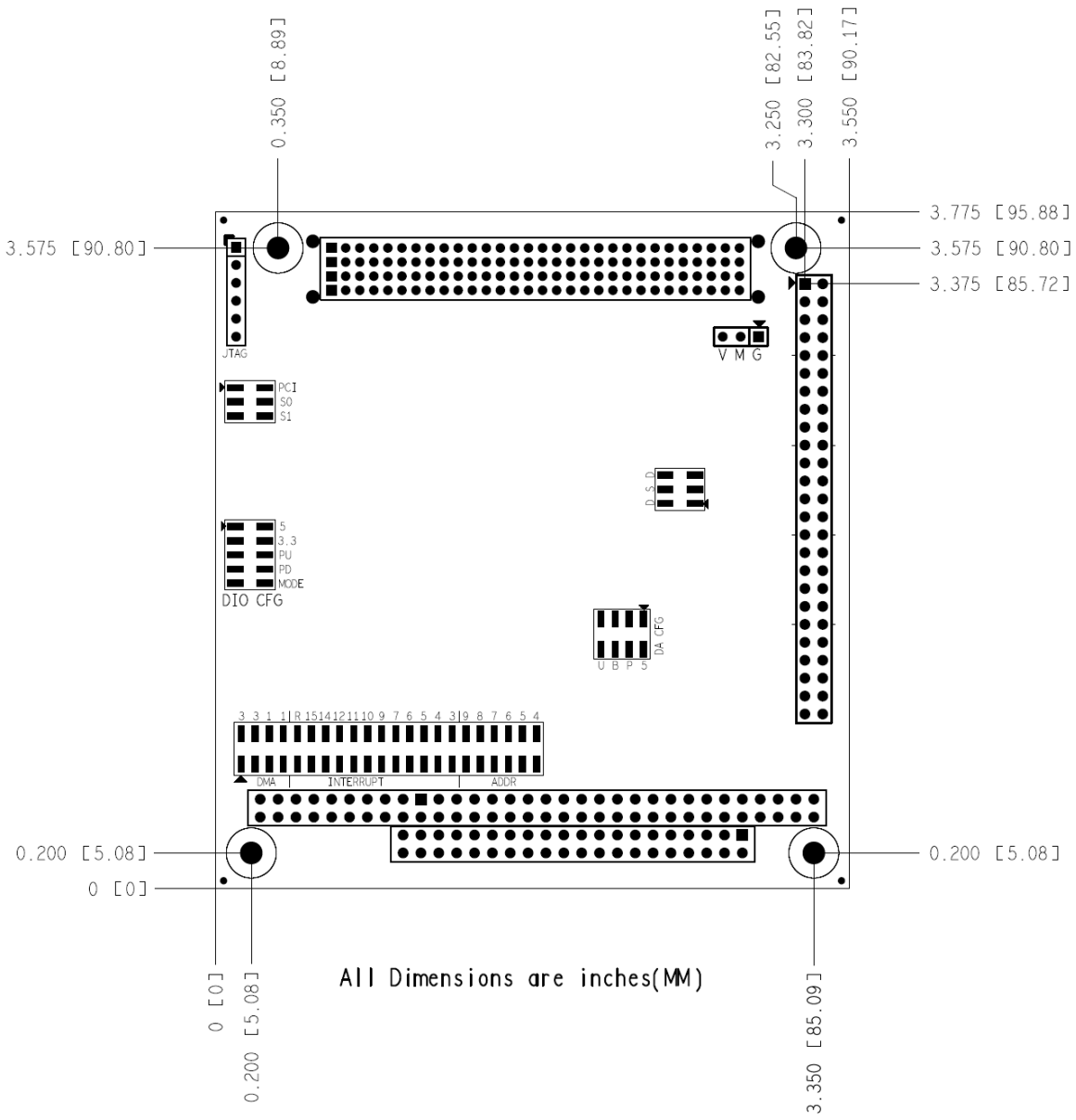


Figure 3 DMM-16R(P)-AT Mechanical Drawing

Feature descriptions

J1	PC/104 8-bit bus connector
J2	PC/104 16-bit bus connector
J3	User I/O connector
J4	A/D single-ended / differential configuration jumper block
J5	D/A range and polarity configuration jumper block
J6	DMA / Interrupt / Address configuration
J7	Factory use calibration connector
J8	Digital I/O configuration jumper block
J9	JTAG connector (normally not used)
J10	PC/104 PCI Connector (DMM-16RP-AT only)
J11	PCI slot configuration jumper block (DMM-16RP-AT only)

I/O CONNECTOR PINOUT AND PIN DESCRIPTION

Diamond-MM-16R-AT provides a 50-pin header labeled J3 for all user I/O. This header is located on the right side of the board. Pin 1 is the upper left pin and is marked on the board.

Vin 15 / 7-	1	2	Vin 7 / 7+
Vin 14 / 6-	3	4	Vin 6 / 6+
Vin 13 / 5-	5	6	Vin 5 / 5+
Vin 12 / 4-	7	8	Vin 4 / 4+
Vin 11 / 3-	9	10	Vin 3 / 3+
Vin 10 / 2-	11	12	Vin 2 / 2+
Vin 9 / 1-	13	14	Vin 1 / 1+
Vin 8 / 0-	15	16	Vin 0 / 0+
Agnd	17	18	Vref Out
Agnd	19	20	Vout 0
Agnd	21	22	Vout 1
Agnd	23	24	+15V
-15V	25	26	Vout 2
Agnd	27	28	Vout 3
In 0-	29	30	Dgnd
Out 0	31	32	Out 2
DIO B7	33	34	DIO B6
DIO B5	35	36	DIO B4
DIO B3	37	38	DIO B2
DIO B1	39	40	DIO B0
DIO A7	41	42	DIO A6
DIO A5	43	44	DIO A4
DIO A3	45	46	DIO A2 / Gate 0
DIO A1	47	48	DIO A0 / Gate 1/2
+5V	49	50	Dgnd

Signal Name	Definition
Vin 7/7+ ~ Vin 0/0+	Analog input channels 7 – 0 in single-ended mode; High side of input channels 7 – 0 in differential mode
Vin 15/7- ~ Vin 8/0-	Analog input channels 15 – 8 in both single-ended mode; Low side of input channels 7 – 0 in differential mode
Vout0-3	Analog output channels 0 – 3
Vref Out	+5V precision reference voltage output; max available current 5mA
DIO B7-0	Digital I/O port B
DIO A7-0	Digital I/O port A
DIO A2 / Gate 0	Digital I/O line A2 doubles as the gate control for counter 0; Counter 0 counts when this line is high and holds when it is low.
DIO A0 / Gate 1/2	Digital I/O line A0 doubles as a gate signal for counters 1 and 2 (32-bit counter) as determined by the control register at base + 11.
In0-	Counter 0 input, negative polarity (negative edge trigger)
Out0, Out2	Counter 0 and Counter 2 output signals
±15V	Analog power supply; maximum available current **10mA** per line; not short circuit protected
+5V	Connected to PC/104 bus power supply; not short circuit protected
Agnd	Analog ground, to be used as a reference for all analog input and output channels; All Agnd pins are tied together on the board.
Dgnd	Digital ground, to be used as a reference for all digital I/O and counter/timer signals

4. BOARD CONFIGURATION

Refer to the Drawing of DMM-16R-AT on Page 5 for locations of the configuration items mentioned here.

4.1 I/O Base Address (ISA bus only)

Each board in the system must have a different base address. In ISA bus mode, the board's base address is set with a portion of jumper block J6, located at the lower left corner of the board. Each of the six jumper locations marked 9, 8, 7, 6, 5, 4 corresponds to the same-numbered address bit in the board's 10-bit I/O address. Bits 3-0 are always 0 for the base address, resulting in a 16-byte I/O address block. A jumper out is equal to a 1, and a jumper in is equal to a 0. Although any 16-byte location is selectable, certain locations are reserved or may cause conflicts with other system resources. The table below lists recommended base address settings for Diamond-MM-16R-AT. The default setting is 300 Hex.

Base Address		**Jumper Position**					
Hex	**Decimal**	**9**	**8**	**7**	**6**	**5**	**4**
220	544	Out	In	In	In	Out	In
240	576	Out	In	In	Out	In	In
250	592	Out	In	In	Out	In	Out
260	608	Out	In	In	Out	Out	In
280	640	Out	In	Out	In	In	In
290	656	Out	In	Out	In	In	Out
2A0	672	Out	In	Out	In	Out	In
2B0	688	Out	In	Out	In	Out	Out
2C0	704	Out	In	Out	Out	In	In
2D0	720	Out	In	Out	Out	In	Out
2E0	736	Out	In	Out	Out	Out	In
300	768 (Default)	Out	Out	In	In	In	In
330	816	Out	Out	In	In	Out	Out
340	832	Out	Out	In	Out	In	In
350	848	Out	Out	In	Out	In	Out
360	864	Out	Out	In	Out	Out	In
380	896	Out	Out	Out	In	In	In
390	912	Out	Out	Out	In	In	Out
3A0	928	Out	Out	Out	In	Out	In
3C0	960	Out	Out	Out	Out	In	In
3E0	992	Out	Out	Out	Out	Out	In

4.2 Slot Selection (DMM-16RP-AT PCI bus only)

When the PCI bus is being used on model DMM-16RP-AT, jumper block J11 is used to select the bus and define which "slot" the board will occupy. Install a jumper in the PCI position to force the board into PCI mode. If the jumper is removed, the board will use the ISA bus instead.

WARNING: DMM-16RP-AT uses an FPGA which contains I/O pins that operate at 3.3V levels are are not 5V tolerant. The board must only be installed on a host SBC that is configured for 3.3V PCI bus signaling.

The PCI slot is selected with jumpers S1 and S0 according to the table. Typically the first PCI-104 board installed on the SBC should be configured for slot 0, the next one for slot 1, and so on. On some SBCs, slot 0 may already be "occupied" with an onboard peripheral circuit such as Ethernet. In this case add 1 to the position to determine the slot number for the board.

J11 PCI configuration

PCI	S1	S0	Configuration
In	In	In	PCI slot 0
In	In	Out	PCI slot 1
In	Out	In	PCI slot 2
In	Out	Out	PCI slot 3
Out	X	X	ISA bus selected

4.3 A/D Single-Ended / Differential Mode

A single-ended input uses 2 wires, input and ground. The measured input voltage is the difference between these two wires. A differential input uses 3 wires: input +, input -, and ground. The measured input voltage is the difference between the + and - inputs.

A differential input has higher noise immunity than a single-ended input, since most noise affects both + and – input wires equally, whereas the noise in the ground signal will be a combination of radiated / conducted noise and noise injected into the ground signal by other electronic components on the board or in the signal source. The downside of differential inputs is that only half as many are available, since two input pins are required to produce a single differential input. DMM-16R-AT can be configured for either 16 single-ended inputs or 8 differential inputs.

Jumper block J4 selects the analog input mode. For single-ended inputs, install a single jumper in the S position. An unused jumper may be stored for later use by installing it over only one pin. For differential inputs, install two jumpers in the two D positions. All input channels are configured in the same mode.

If you have a combination of single-ended and differential input signals, select differential mode. Then to measure the single-ended signals, connect the input signal to the + input and connect analog ground to the - input.

4.4 J5: D/A Configuration

The 4 D/A channels can be configured in two ways:

- The full-scale output range can be selected between a fixed +5V output range or a user-programmable output range. The programmable range can be set anywhere between 1V and 10V.

- The outputs can be configured for unipolar (positive voltages only) or bipolar (both negative and positive output voltages). In unipolar mode, the outputs range from 0V minimum to the selected full-scale voltage (e.g. 5V in the fixed range). In bipolar mode, the outputs can range from – full-scale voltage to + full-scale voltage (e.g. +/-5V in the fixed range). Note that the maximum swing in bipolar mode is equal in both directions.

Two jumpers in J5 are used to configure the D/A channels. For fixed range, install a jumper in the location marked 5. For programmable range, install a jumper in the location marked P. Do not install a jumper in both locations simultaneously or across the two columns, as unpredictable behavior may result.

For bipolar inputs, install a jumper in the B location. For unipolar inputs, install a jumper in the U location. Do not install a jumper in both locations simultaneously or across the two columns, as unpredictable behavior may result.

Both the range and polarity jumpers must be installed for proper analog output behavior.

4.5 Interrupt Level Selection (for ISA bus interface only)

Jumper block J6 is used to configure interrupt level for ISA bus operation.

Interrupts are used to transfer data from the board to memory at a rate higher than that can be achieved through software sampling. During interrupt operation, the board will periodically generate an interrupt request. The processor will respond and run a user-supplied interrupt routine function (or the function supplied with the board's driver software). The interrupt routine reads the data from the board and makes it available to the user application program.

DMM-16R-AT allows you to select from levels 15, 14, 12, 11, 10, 9, 7, 6, 5, 4, and 3. Only one IRQ level is used by DMM-16R-AT. To select the desired IRQ level install a jumper in that number's location in the Interrupt area of jumper block J6.

On the PC/104 bus each IRQ level in use must have a 1KΩ pull-down resistor attached. To enable the pull-down resistor for this board, install a jumper in the R location on J6.

Typically, each peripheral board in a PC/104 system will use a different interrupt level, or IRQ level. However, in special circumstances multiple boards may share the same IRQ level. In this case only one board should have the pull-down resistor enabled with the R jumper. The other boards should not have the resistor enabled.

5. I/O REGISTER MAP

5.1 Overview

DMM-16R-AT occupies 16 bytes in I/O space. For ISA bus operation, these registers are located in the ISA bus I/O address space. For PCI bus operation, these registers are located in the BAR0 configured during system boot.

A functional list of these registers is provided below, and detailed bit definitions are provided on the next page and the following chapter.

Base +	Write Function	Read Function
0	Start A/D conversion	A/D LSB
1	D/A LSB	A/D MSB
2	A/D channel register	A/D channel register
3	Digital output port	Digital input port
4	D/A 0 MSB	Update D/A
5	D/A 1 MSB	Update D/A
6	D/A 2 MSB	Update D/A
7	D/A 3 MSB	Update D/A
8	Clear interrupt flip flop	Status register
9	Interrupt control register	Interrupt control register readback
10	Ctr/Timer and FIFO Control Register	FIFO / status register
11	Analog Configuration Register	Analog and FIFO register readback

Addresses 12-15 form a window into two 4-byte pages. Addresses 10-15 constitutes the extended page of 6 bytes. The page is selected with bits in registers 8 and 10.

Page 0: 82C54 counter/timer

12	Counter/timer 0 data register	Counter/timer 0 data register
13	Counter/timer 1 data register	Counter/timer 1 data register
14	Counter/timer 2 data register	Counter/timer 2 data register
15	Counter/timer control register	Counter/timer control register

Page 1: Calibration Control

12	EEPROM / TrimDAC data register	EEPROM / TrimDAC data register
13	EEPROM / TrimDAC address register	EEPROM / TrimDAC address register
14	Calibration control register	Calibration status register
15	EEPROM access key	FPGA code version

Page 2 (extended page): Digital I/O Control and FIFO

10		FIFO Depth Register 7 -0
11		FIFO Depth Register 9 - 8
12	Port A output data	Port A input data
13	Port B output data	Port B input data
14	LED control	LED and FIFO status
15	Port direction control	Port direction control readback

5.2 Register Map Bit Assignments

A blank location in the Write registers has no function.

A blank location in the Read registers has no function and reads back as 0.

WRITE operations

	7	6	5	4	3	2	1	0
0	Start A/D Conversion							
1	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
2	HIGH3	HIGH2	HIGH1	HIGH0	LOW3	LOW2	LOW1	LOW0
3	DOUT7	DOUT6	DOUT5	DOUT4	DOUT3	DOUT2	DOUT1	DOUT0
4					DA0-11	DA0-10	DA0-9	DA0-8
5					DA1-11	DA1-10	DA1-9	DA1-8
6					DA2-11	DA2-10	DA2-9	DA2-8
7					DA3-11	DA3-10	DA3-9	DA3-8
8		EXTPG	EXTEN1	EXTEN0	CLRINT			
9	AINTE				TINTE	RSVD	CLKEN	CLKSEL
10	FIFORST	PAGE	FIFOEN	SCANEN	CLKFRQ	C2	C1	C0
11				SCNINT	RANGE	ADBU	G1	G0
12	See next page							
13	See next page							
14	See next page							
15	See next page							

READ operations

	7	6	5	4	3	2	1	0
0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
1	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
2	HIGH3	HIGH2	HIGH1	HIGH0	LOW3	LOW2	LOW1	LOW0
3	DIN7	DIN6	DIN5	DIN4	DIN3	DIN2	DIN1	DIN0
4	Update D/A							
5	Update D/A / read back FPGA revision code							
6	Update D/A / readback FPGA new ID minor byte							
7	Update D/A / readback FPGA new ID major byte							
8	STS	TINT	SD	AINT	CH3	CH2	CH1	CH0
9	AINTE	EXTPG	PAGE	DMODE	TINTE	DMAEN	CLKEN	CLKSEL
10 *	WAIT	PAGE	FIFOEN	SCANEN	CLKFRQ	OVF	HF	EF
11 *	C2	C1	C0		RANGE	ADBU	G1	G0
12	See next page							
13	See next page							
14	See next page							
15	See next page							

* Registers 10 and 11 are the same for pages 0 and 1 but different for page 2. See below.

Page 0

Page 0 is used to access the 82C54 counter/timer core in the FPGA.

WRITE and READ operations:

Bit no.	7	6	5	4	3	2	1	0
12	Ctr0D7	Ctr0D6	Ctr0D5	Ctr0D4	Ctr0D3	Ctr0D2	Ctr0D1	Ctr0D0
13	Ctr1D7	Ctr1D6	Ctr1D5	Ctr1D4	Ctr1D3	Ctr1D2	Ctr1D1	Ctr1D0
14	Ctr2D7	Ctr2D6	Ctr2D5	Ctr2D4	Ctr2D3	Ctr2D2	Ctr2D1	Ctr2D0
15	SC1	SC0	RW1	RW0	M2	M1	M0	BCD

Page 1

Page 1 is used to manage the autocalibration features.

WRITE operations:

Bit no.	7	6	5	4	3	2	1	0
12	D7	D6	D5	D4	D3	D2	D1	D0
13	A7	A6	A5	A4	A3	A2	A1	A0
14	EE_EN	EE_RW	RUNCAL	CMUXEN	TDACEN			
15	EEPROM access code							

READ operations:

Bit No.	7	6	5	4	3	2	1	0
12	D7	D6	D5	D4	D3	D2	D1	D0
13	A7	A6	A5	A4	A3	A2	A1	A0
14	0	TDBUSY	EEBUSY	CMUXEN	TDACEN	0	0	0
15	FPGA ID							

Page 2

Page 2 is used to manage the enhanced mode FIFO, digital I/O, and user LED features.

Registers 10 and 11 are the same in write mode for all pages, but they are different in read mode for page 2. Therefore they are included in the Read operation table below.

WRITE operations:

Bit no.	7	6	5	4	3	2	1	0
12	A7	A6	A5	A4	A3	A2	A1	A0
13	B7	B6	B5	B4	B3	B2	B1	B0
14		LED						
15							DIRB	DIRA

READ operations:

Bit no.	7	6	5	4	3	2	1	0
10	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
11							FD9	FD8
12	A7	A6	A5	A4	A3	A2	A1	A0
13	B7	B6	B5	B4	B3	B2	B1	B0
14		LED		UF	OF	FF	HF	EF
15							DIRB	DIRA

6. REGISTER DEFINITIONS

Base + 0 Read A/D LSB

Bit No.	7	6	5	4	3	2	1	0
Name	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

Definitions:

AD7 – 0 A/D data bits 7 - 0; AD0 is the LSB; A/D data is a signed 16-bit value ranging from -32768 to +32767.

Base + 0 Write Start A/D Conversion

Writing to Base + 0 starts an A/D conversion. The value written does not matter.

Base + 1 Read A/D MSB

Bit No.	7	6	5	4	3	2	1	0
Name	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8

Definitions:

AD15 – 8 A/D data bits 15-8; AD15 is the MSB

Note: Reading from Base + 0 and Base + 1 result in the same physical operation, reading from the FIFO.

The FIFO is 8 bits wide, with A/D data stored and retrieved in interleaved fashion. Data from the A/D is put into the FIFO in little-endian mode, with the LSB inserted first, and the MSB inserted second. Thus the data comes out of the FIFO in the same order. Each time a byte is read from either Base + 0 or Base + 1, the next byte will be read from the FIFO and the FIFO counter will be decremented.

Because the FIFO decrements after each read operation, you cannot read the same value more than once (unless the FIFO is empty, in which case the last byte may be read indefinitely). It is the programmer's responsibility to ensure that data is read out of the FIFO properly so that appropriate pairs of bytes are read out together.

Base + 1 Write D/A LSB

Bit No.	7	6	5	4	3	2	1	0
Name	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0

Definitions:

DA7-0 D/A bits 7-0; DA0 is the LSB. D/A data is an unsigned 12-bit number ranging from 0 to 4095.

Base + 2 Read/Write A/D Channel Register

Bit No.	7	6	5	4	3	2	1	0
Name	HIGH3	HIGH2	HIGH1	HIGH0	LOW3	LOW2	LOW1	LOW0

Definitions:

HIGH3 – 0 High channel of channel scan range

Ranges from 0 to 15 in single-ended mode, 0 - 7 in differential mode.

LOW3 – 0 Low channel of channel scan range

Ranges from 0 to 15 in single-ended mode, 0 - 7 in differential mode.

The high channel must be greater than or equal to the low channel.

When this register is written, the current A/D channel is set to the low channel.

A/D channels are automatically selected in sequence by the board. Each time an A/D conversion (A/D sample) starts, the board increments to the next channel in the range. When the high channel is sampled, the board resets to the low channel.

Base + 3 Write Digital Output Port (ISA Legacy mode)

Bit No.	7	6	5	4	3	2	1	0
Name	DIOB7	DIOB6	DIOB5	DIOB4	DIOB3	DIOB2	DIOB1	DIOB0

When DMM-16R-AT is configured for Legacy DIO mode, port B is fixed as output, and this register is used to write data to it. Port B is on I/O connector J3 pins 41-48. In Enhanced mode, this register is not used.

On power-up or reset, the output register is cleared to all zeroes.

Base + 3 Read Digital Input Port (ISA Legacy mode)

Bit No.	7	6	5	4	3	2	1	0
Name	DIOA7	DIOA6	DIOA5	DIOA4	DIOA3	DIOA2	DIOA1	DIOA0

When DMM-16R-AT is configured for Legacy DIO mode, port A is fixed as input, and this register is used to read data from it. Port A is on I/O connector J3 pins 33-40. In Enhanced mode, this register is not used.

Alternate Functions (see Counter/Timer Operation Chapter)

DIN0	External A/D trigger
DIN2	Counter 0 Gate Input

Base + 4 through Base + 7 Write DAC 0 – 3 MSB

Bit No.	7	6	5	4	3	2	1	0
Name					DA11	DA10	DA9	DA8

Definitions:

DA11 – 8 D/A data bits 11 – 8 for the selected channel. DA11 is the MSB.

Base + 4 is used for D/A 0, Base + 5 is used for D/A 1, Base + 6 is used for D/A 2, and Base + 7 is used for D/A 3.

The final D/A value is constructed of the 4 upper bits written to these registers combined with the 8 lower bits of the D/A value written to Base + 1. Writing data to any of these 4 registers causes these 4 bits and the 8 lower bits from Base + 1 to be transferred to the selected D/A channel. However the D/A is not updated until a read operation is performed on one of these 4 addresses. This lets you write data to more than one D/A and then update all of them at the same time.

Since the Base + 1 register is shared by all 4 D/A channels, each D/A channel must have its data written in the proper sequence. First write the LSB to Base + 1, then write the MSB to one of the MSB registers 4-7 depending on the D/A selected. Repeat these two writes for each D/A you want to update. After all data is written, read from any of these registers to update all the D/A channels simultaneously.

Note that even though all channels are updated simultaneously, a channel will only change if it has new data written to it since the last update operation. Otherwise it will maintain its present value during the update operation.

Base + 4 through Base + 7 Read Update D/A channels / read FPGA ID and revision

Reading from any of these 4 addresses will cause the 4 analog outputs to be updated. All outputs are updated simultaneously. See detailed description above.

Register 7 reads back the FPGA major ID for this design, 0x14.
Register 6 reads back the FPGA minor ID for this design, 0x01.
Register 5 reads back the FPGA revision. This starts with 0x01 and increments with each successive version of the FPGA.
Registers 4 reads back as 0x00 always.

Base + 8 **Write Clear Interrupt Request Flip Flop**

Bit No.	7	6	5	4	3	2	1	0
Name		EXTPG	EXTEN1	EXTEN0	CLRINT			

EXTEN1-0 Extended page (page 2) enable

These bits are used to select whether EXTPG will be updated. If EXTEN1-0 = 1 0, then EXTPG is updated with the value in bit 6 during a write to this register, and CLRINT is not updated. If EXTEN1-0 is any value other than 1 0, the EXTPG bit is not updated during a write to this register, and CLRINT is updated.

EXTPG Extended page; active only if EXTEN1-0 = 1 0

1 Select extended page (page 2) at base + 10-15 (PAGE bit is ignored)

0 Select normal page operation at base + 10-15 (page is selected with PAGE bit)

CLRINT Clear interrupt request; active only if EXTEN1-0 <> 1 0

1 Clear interrupt request flip flop

0 No action

Base + 8 **Read** **Status Register**

Bit No.	7	6	5	4	3	2	1	0
Name	STS	TINT	SD	AINT	ADCH3	ADCH2	ADCH1	ADCH0

STS A/D chip status:

1 A/D conversion or scan is in progress

0 A/D is idle

TINT Timer interrupt request status:

1 Interrupt request has been generated by timer 0

0 No interrupt is pending from timer 0

SD Single-ended / Differential A/D input mode setting (readback of jumper setting):

1 Single-ended (default)

0 Differential

AINT Analog interrupt request status:

1 Interrupt request is pending from A/D circuit

0 No interrupt is pending from A/D circuit

ADCH3 - 0 Current A/D channel; this is the channel currently selected on board and is the channel that will be used for the next A/D conversion (unless a new value is written to the channel register before then).

Base + 9 **Write** **Control Register**

Bit No.	7	6	5	4	3	2	1	0
Name	AINTE				TINTE	RSVD	CLKEN	CLKSEL

AINTE Analog interrupt enable:

1 Enable A/D interrupts

0 Disable A/D interrupts

TINTE Timer interrupt enable:

1 Enable interrupts from timer 0

0 Disable interrupts from timer 0

⇒**:** Both AINTE and TINTE should not be set concurrently. Only one interrupt operation at a time is supported by the board.

RSVD DMA enable (reserved for future implementation, not currently supported)

CLKEN Enable hardware A/D clock:

1 Enable hardware A/D trigger (source is selected with CLKSEL bit); software triggers are disabled

0 Disable hardware trigger; A/D is triggered via software write to Base + 0

CLKSEL A/D clock select, used only when CLKEN = 1:

1 Internal trigger: Counter/timer (82C54) generates A/D conversions

0 External trigger: PA0, pin 48 on I/O connector J3, generates A/D conversions. This feature would work only if Port A is input port.

Base + 9 **Read** **Control readback**

Bit No.	7	6	5	4	3	2	1	0
Name	AINTE	EXTPG	PAGE	DMODE	TINTE	RSVD	CLKEN	CLKSEL

This register may be used to read the values of various control bits described above. Note that the PAGE bit is duplicated here and in register 10. If EXTPG = 0, then the PAGE bit reads back the current page setting 0 or 1. If EXTPG = 1, then the FPGA is forced into page 2 and PAGE reads back as 0. However its register contents are preserved, so that later when EXTPG returns to 0 the page returns to its previous setting of 0 or 1.

DMODE Digital I/O Mode selection; this determines if the DIO ports function in legacy mode or enhanced mode. Pin P_DMODE along with the active host bus determine the value of DMODE as follows:

Bus	P_DMODE	DMODE	Meaning
ISA	0	0	Legacy
ISA	1	1	Advanced
PCI	X	1	Advanced

0 Legacy Mode: Port A is in fixed input mode, and pins PA7-0 are set to input. Port B is in fixed output mode, and pins PB7-0 are set to output. P_DIRA = 0 and P_DIRB= 1.

1 Enhanced Mode: The direction of PA7-0 and PB7-0, and pins P_DIRA and P_DIRB, are determined by register bits DIRA and DIRB

Base + 10 Write Counter/Timer and FIFO Control Register (all pages)

Bit No.	7	6	5	4	3	2	1	0
Name	FIFORST	PAGE	FIFOEN	SCANEN	CLKFRQ	C2	C1	C0

FIFORST Reset FIFO. Writing a 1 to this bit causes the on-board FIFO to be reset to empty in preparation for an interrupt-based A/D operation. If this register is written to with a 1 in this bit, the board will ignore the other 7 bits of the written value, and the current values of the other 7 bits in the register will be preserved.

PAGE Page number for registers at Base + 12 through Base + 15

Page 0: 82C54 counter/timer access

Page 1: Calibration registers

FIFOEN FIFO enable:

1 Enable FIFO operation; if interrupts are enabled, interrupt requests will occur when the FIFO reaches or exceeds half-full (HF = 1).

0 Disable FIFO operation; if interrupts are enabled, interrupts will occur after each A/D conversion or scan is completed.

SCANEN Scan enable:

1 A/D scan mode enabled; FIFO will fill up with data for a single scan, and STS will stay high until an entire scan is complete. If interrupts are enabled, interrupts will occur on integral multiples of scans.

0 Scan mode disabled; the STS bit will remain high for a single conversion

CLKFRQ Clock frequency for counter/timer 1

0 10MHz

1 1MHz

C2 External Clock Gate Enable

1 IN0- (pin 29 on the I/O header) acts as a gate for A/D sample control when external A/D clock is enabled (CLKSEL = 0 above). When IN0- is high, falling edges on DI0 (pin 48 on the I/O header) will initiate A/D conversions. When IN0- is low, the DI0 signal is inhibited. IN0- is connected to a 10KΩ pull-up resistor.

0 IN0- does not act as a gate for external A/D clocking.

C1 Counter 0 input source:

1 Input to Counter 0 is a 100kHz on-board reference frequency derived from the 10MHz oscillator. IN0- (pin 29 on the I/O header) gates this signal. When it is high (default), the 100kHz signal runs. When it is low, the 100kHz signal is stopped.

0 Input to Counter 0 is IN0- (pin 29 on the I/O connector) inverted. Counter 0 counts on rising edges of IN0-. IN0- is connected to an on-board pull-up resistor, so only a connection to ground is necessary to toggle it.

C0 Counters 1 and 2 gate control:

1 Counters 1 and 2 are gated by DIN0 (pin 48 on the I/O connector). When DIN0 is high, the counters run; when DI0 is low, the counters are stopped. In this way pin 48 can be used as an A/D conversion gate signal when the counters are used for A/D conversion timing.

0 Counters 1 and 2 run freely with no gating.

Base + 10 Read Counter/Timer and FIFO Status Register (pages 0 and 1 only)

Bit No.	7	6	5	4	3	2	1	0
Name	WAIT	PAGE	FIFOEN	SCANEN	CLKFRQ	OVF	HF	EF

WAIT Analog input circuit status. Whenever register 2 (channel register) or 11 (input range register) is written to, WAIT will go high for approximately 10μS as the circuit adjusts to the new signal.

1 The analog input circuit is busy settling on a new signal. Do not perform A/D conversions when WAIT = 1.

0 The circuit is ready for A/D conversions

PAGE Readback of PAGE bit described on previous page. If EXTPG = 0, then the PAGE bit reads back the current page setting 0 or 1. If EXTPG = 1, then the FPGA is forced into page 2, and PAGE reads back as 0. However its register contents are preserved, so that later when EXTPG returns to 0 the page returns to its previous setting of 0 or 1.

FIFOEN Readback of FIFOEN bit described on previous page

SCANEN Readback of SCANEN bit described on previous page

CLKFRQ Readback of CLKFRQ bit described on previous page

OVF FIFO overflow flag; 0 = no overflow; 1 = overflow

Overflow is defined as the state when the FIFO is full and another A/D conversion occurs before any data is read out of the FIFO. In an overflow condition the FIFO contents are preserved, and no new data will be written to the FIFO. To clear an overflow condition, the FIFO must be reset with the FIFORST bit in register 10.

HF FIFO half full flag; 0 = FIFO is less than half full; 1 = FIFO is at least half full

EF FIFO empty flag; 0 = FIFO is not empty; 1 = FIFO is empty

Additional FIFO flags OF (overflow) and UF (underflow are accessible in page 2.

Base + 11 Write Analog Configuration Register (all pages)

Bit No.	7	6	5	4	3	2	1	0
Name				SCNINT	RANGE	ADBU	G1	G0

SCNINT Scan interval. This is the time between A/D samples during an A/D scan. An A/D scan occurs when SCANEN = 1 (Base + 10 bit 4) and an A/D conversion is triggered.

0 9.3µS

0 5.3µS

RANGE 5V or 10V A/D positive full-scale range; 0 = 5V, 1 = 10V

ADBU A/D bipolar / unipolar setting; 0 = bipolar, 1 = unipolar

The table below lists the various combinations of ADBU and RANGE. The numbers shown are NOT the same as the input voltage range. See G1-0 below.

RANGE	ADBU	A/D full-scale range
0	0	±5V
0	1	Invalid setting
1	0	±10V
1	1	0–10V

G1 – 0 A/D gain setting:

G1	G0	Gain
0	0	1
0	1	2
1	0	4
1	1	8

The gain setting is the ratio between the A/D full-scale range shown above and the effective input signal range. For example, if the A/D full-scale range is 0–10V, a gain setting of 2 creates an input signal range of 0 – 5V, and a gain setting of 4 creates an input signal range of 0 – 2.5V.

⇒**:** On power up or system reset, the board is configured for A/D bipolar mode, input range ±5V, gain = 1 (this register is cleared to 0).

Base + 11 Read Analog and Status Readback Register (pages 0 and 1 only)

Bit No.	7	6	5	4	3	2	1	0
Name	C2	C1	C0		RANGE	ADBU	G1	G0

This address provides a means of reading back the values written to the registers at Base + 10 (C2, C1, C0) and Base + 11 (RANGE, ADBU, G1, G0).

PAGE 0: 82C54 Counter/Timer

Base + 12 through Base + 15 Read/Write Counter/Timer Registers

These registers access the internal 82C54 counter/timer core.

Base + 12 Read/ Write Counter 0 Data register

Bit No.	7	6	5	4	3	2	1	0
Name	Ctr0D7	Ctr0D6	Ctr0D5	Ctr0D4	Ctr0D3	Ctr0D2	Ctr0D1	Ctr0D0

Base + 13 Read/ Write Counter 1 Data register

Bit No.	7	6	5	4	3	2	1	0
Name	Ctr1D7	Ctr1D6	Ctr1D5	Ctr1D4	Ctr1D3	Ctr1D2	Ctr1D1	Ctr1D0

Base + 14 Read/ Write Counter 2 Data register

Bit No.	7	6	5	4	3	2	1	0
Name	Ctr2D7	Ctr2D6	Ctr2D5	Ctr2D4	Ctr2D3	Ctr2D2	Ctr2D1	Ctr2D0

Base + 15 Read/ Write Counter Control register

Bit No.	7	6	5	4	3	2	1	0
Name	SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC1-0 Select Counter 1 - 0

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Read Back command

RW1-0 Read/ Write

RW1	RW0	
0	0	Counter Latch command
0	1	Read/ Write LSB only
1	0	Read/ Write MSB only
1	1	Read/ Write LSB first, then MSB

M2-0 Mode

The counter has 6 modes Mode 0-5.

M2	M1	M0	
0	0	0	Mode 0: Interrupt on terminal count
0	0	1	Mode 1: Hardware retrigger able one shot
x	1	0	Mode 2: Rate generator
x	1	1	Mode 3: Square wave mode
1	0	0	Mode 4: Software triggered mode
1	0	1	Mode 5: Hardware triggered strobe

Page 1: Calibration Control Registers

Base + 12 Read/Write EEPROM / TrimDAC Data Register

Bit No.	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0

D7-0 Calibration data to be read or written to the EEPROM and/or TrimDAC.

During EEPROM or TrimDAC write operations, the data written to this register will be written to the selected device.

During EEPROM read operations this register contains the data to be read from the EEPROM and is valid after CALSTS = 0.

The TrimDAC data cannot be read back.

Base + 13 Read/Write EEPROM / TrimDAC Address Register

Bit No.	7	6	5	4	3	2	1	0
Name	A7	A6	A5	A4	A3	A2	A1	A0

A7-A0 EEPROM / TrimDAC address. The EEPROM recognizes address 0 – 127 using address bits A6 – A0. The TrimDAC only recognizes addresses 0 – 7 using bits A2 – A0. In each case remaining address bits will be ignored.

Base + 14 Write Calibration Control Register

Bit No.	7	6	5	4	3	2	1	0
Name	EE_EN	EE_RW	RUNCAL	CMUXEN	TDACEN			

This register is used to initiate various commands related to autocalibration. More detailed information on autocalibration may be found elsewhere in this manual.

EE_EN EEPROM Enable. Writing a 1 to this bit will initiate a transfer to/from the EEPROM as indicated by the EE_RW bit.

EE_RW Selects read or write operation for the EEPROM: 0 = Write, 1 = Read.

RUNCAL Writing 1 to this bit causes the board to reload the calibration settings from EEPROM.

CMUXEN Calibration multiplexor enable. Pin P_MUXEN2 equals value of CMUXEN. When CMUXEN = 1, P_MUXEN1,0 should be set to 0. When CMUXEN = 0, P_MUXEN1, 0 should be set to 1

TDACEN TrimDAC Enable. Writing 1 to this bit will initiate a transfer to the TrimDAC (used in the auto calibration process).

Base + 14 Read Calibration Status Register

Bit No.	7	6	5	4	3	2	1	0
Name	0	TDBUSY	EEBUSY	CMUXEN	TDACEN	0	0	0

TDBUSY TrimDAC busy indicator

0 User may access TrimDAC

1 TrimDAC is being accessed; user must wait

EEBUSY EEPROM busy indicator

0 User may access EEPROM

1 EEPROM is being accessed; user must wait

Base + 15 Write EEPROM Access Key Register

The user must write the value 0xA5 (binary 10100101) to this register each time after setting the PAGE bit in order to get access to the EEPROM. This helps prevent accidental corruption of the EEPROM contents.

Base + 15 Read FPGA Revision Code

This register may be read back to indicate the revision level of the FPGA design. This value matches the original DMM-16-AT value to ensure backward compatibility.

Page 2 (extended page): Digital I/O Control and FIFO

Base + 10 Read FIFO Depth bits 7 -0

Bit No.	7	6	5	4	3	2	1	0
Name	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0

Base + 11 Read FIFO Depth bit 8

Bit No.	7	6	5	4	3	2	1	0
Name							FD9	FD8

This 10-bit value indicates the current number of samples in the A/D FIFO, 0 to 512. This register is cleared to 0 when the FIFO is reset.

Base + 12 Read/Write DIO port A (Enhanced mode)

Bit No.	7	6	5	4	3	2	1	0
Name	DIOA7	DIOA6	DIOA5	DIOA4	DIOA3	DIOA2	DIOA1	DIOA0

A7-0 Digital I/O port A data

When DIO Enhanced mode is selected, this register is used to read/write data to port A.

Alternate Functions (see Counter/Timer Operation Chapter)

A0 External A/D trigger

A2 Counter 0 Gate Input

Alternate functions are available only when port A is configured as input port (DIRA = 0).

Base + 13 Read/Write DIO port B (Enhanced mode)

Bit No.	7	6	5	4	3	2	1	0
Name	DIOB7	DIOB6	DIOB5	DIOB4	DIOB3	DIOB2	DIOB1	DIOB0

B7-0 Digital I/O port B data

When DIO Enhanced mode is selected, this register is used to read/write data to port B.

When reading these two registers, the value of the corresponding FPGA pins is always returned. In input mode, the pins are driven by the I/O connector. In output mode, the pins are driven by the values in these registers.

Base + 14 Write LED control

Bit No.	7	6	5	4	3	2	1	0
Name		LED						

LED User LED (Blue); 1 = LED ON and 0 = LED OFF. Output pin P_LED is the opposite of the value of this bit. This bit resets to 1.

Base + 14 Read FIFO / LED status

Bit No.	7	6	5	4	3	2	1	0
Name		LED		UF	OF	FF	HF	EF

UF Underflow flag indicates that an attempt was made to read data out of the FIFO when it was empty. When EF = 1 and a read occurs, UF = 1. UF is persistent: It is only reset to 0 on a FIFO reset or when this register is read

OF FIFO overflow flag; 0 = no overflow; 1 = overflow

Overflow is defined as the state when the FIFO is full and another A/D conversion occurs before any data is read out of the FIFO. In an overflow condition the FIFO contents are preserved, and no new data will be written to the FIFO. To clear an overflow condition, the FIFO must be reset with the FIFORST bit in register 10.

FF FIFO full flag; set to 0 when the FIFO is not full and 1 when the FIFO is full

HF FIFO half full flag; 0 = FIFO is less than half full; 1 = FIFO is at least half full

EF FIFO empty flag; 0 = FIFO is not empty; 1 = FIFO is empty

OVF, HF and EF are duplicate register bits, they are also defined in register 10

Base + 15 Read/Write DIO direction control (Enhanced mode)

Bit No.	7	6	5	4	3	2	1	0
Name							DIRB	DIRA

DIRA Digital I/O port A direction control; 1 = output, 0 = input

DIRB Digital I/O port B direction control; 1 = output, 0 = input

When DIO Enhanced mode is selected, this register is used to set the direction for DIO ports A and B. On power-up or reset, the board will automatically configure port A for input and port B for output. The application software can then changes the settings as needed.

7. ANALOG INPUT CIRCUIT DESCRIPTION

7.1 Resolution

DMM-16R-AT uses a 16-bit A/D converter. This means that the analog input voltage can be measured to the precision of a 16-bit binary number. The maximum value of a 16-bit binary number is 2^{16} - 1, or 65535, so the full range of numerical values provided by a 16-bit A/D converter is 0 - 65535.

The smallest change in input voltage that can be detected is $1/(2^{16})$, or 1/65536, of the full-scale input range. This smallest change results in an increase or decrease of 1 in the A/D code, and so this change is referred to as 1 LSB, or 1 least significant bit.

7.2 Unipolar and Bipolar Inputs

Diamond-MM-16R-AT can measure both unipolar (positive only) and bipolar (positive and negative) analog voltages. In general you should select the highest gain (smallest input range) that will allow the A/D converter to read the full range of voltages for your input signals. However, if you pick too high a gain, then the A/D converter will clip at either the high end or low end, and you will not be able to read the full range of input voltages.

7.3 Single Ended and Differential Inputs

Diamond-MM-16R-AT can handle both single-ended and differential inputs. A single-ended input is a two-wire input (one input signal and ground) that is referenced to analog ground on the board. This means that the input voltage will be measured with respect to the board's analog ground. A differential input is a three-wire input (input +, input -, and ground), and the board will measure the difference between the voltages of the two inputs. Polarity is important for a differential input. Diamond-MM-16R-AT will subtract the voltage on the low (-) input from the voltage of the high (+) input. Differential inputs are frequently used when the grounds of the input device and the measurement device (Diamond-MM-16R-AT) are at different voltages, or when a low-level signal is being measured that has its own ground wire. Differential inputs also provide better noise immunity than single-ended inputs, because most of the noise will be present in equal amounts on both the + and – inputs, so in the subtraction process the noise will be cancelled out.

7.4 Input Ranges and Resolution

Range	ADBU	G1	G0	Input Range	Resolution (1 LSB)
0	0	0	0	±5V	153µV
0	0	0	1	±2.5V	76µV
0	0	1	0	±1.25V	38µV
0	0	1	1	±0.625V	19µV
0	1	0	0	Invalid setting	
0	1	0	1	Invalid setting	
0	1	1	0	Invalid setting	
0	1	1	1	Invalid setting	
1	0	0	0	±10V	305µV
1	0	0	1	±5V	153µV
1	0	1	0	±2.5V	76µV
1	0	1	1	±1.25V	38µV
1	1	0	0	0 – 10V	153µV
1	1	0	1	0 – 5V	76µV
1	1	1	0	0 – 2.5V	38µV
1	1	1	1	0 – 1.25V	19µV

7.5 Analog Input Wiring

All analog input signals should use one of the analog ground pins on the I/O connector (Agnd) as their common reference. Connecting the – input of the analog signal to digital ground will induce significant noise in the measurement and lower the measurement accuracy to approximately 8-10 bits. For lowest noise, use shielded wiring when possible, keep the wiring as short as possible, and avoid running analog signals in parallel with noisy power and digital signals or directly over noisy power and digital circuits. Sharing one Agnd pin among several analog inputs is acceptable and will not degrade measurements.

8. PERFORMING AN A/D CONVERSION

This chapter describes the steps involved in performing an A/D conversion on a selected input channel using direct programming (not with the driver software).

There are five steps involved in performing an A/D conversion:

1. **Select the input channel**
2. **Select the input range**
3. **Wait for analog input circuit to settle**
4. **Trigger an A/D conversion**
5. **Wait for the conversion to finish**
6. **Read the data from the board**
7. **Convert the numerical data to a meaningful value**

8.1 Select the input channel

To select the input channel to read, write a low-channel/high-channel pair to the channel register at base + 2. (See register map details earlier in this manual). The low 4 bits select the low channel, and the high 4 bits select the high channel. When you write any value to this register, the current A/D channel is set to the low channel.

For example:

To set the board to channel 4 only, write 0x44 to Base + 2.

To set the board to read channels 0 through 15, write 0xF0 to Base + 2.

⇒ **Note:** When you perform an A/D conversion, the current channel is automatically incremented to the next channel in the selected range. Therefore, to perform A/D conversions on a group of consecutively-numbered channels, you do not need to write the input channel prior to each conversion. For example, to read from channels 0 - 2, write Hex 20 to base + 2. The first conversion is on channel 0, the second will be on channel 1, and the third will be on channel 2. Then the channel counter wraps around to the beginning again, so the fourth conversion will be on channel 0 again and so on.

If you are sampling the same channel repeatedly, then you set both high and low to the same value as in the first example above. Then on subsequent conversions you do not need to set the channel again.

8.2 Select the input range

Select the input range from among the available ranges shown above. If the range is the same as for the previous A/D conversion then it does not need to be set again. Write this value to the input range register at Base + 11.

For example:

For ±10V range, write 0x08 to Base + 11.

8.3 Wait for analog input circuit to settle

After writing to either the channel register (Base + 2) or the input range register (Base + 11), you must allow time for the analog input circuit to settle before starting an A/D conversion. The board has a built-in 10μS timer to assist with the wait period. Monitor the WAIT bit at Base + 10 bit 7. When it is 1 the circuit is actively settling on the input signal. When it is 0 the board is ready to perform A/D conversions.

8.4 Trigger and A/D conversion

After the above steps are completed, start the A/D conversion by writing to Base + 0. This write operation only triggers the A/D if the CLKEN bit is 0 to disable hardware triggering and enable software triggering. Otherwise the A/D will only trigger when the selected clock or trigger signal occurs. CLKEN should always be 0 when controlling A/D conversions in software.

8.5 Wait for the conversion to finish

The A/D converter takes up to 10 microseconds to complete a conversion. Most processors and software can operate fast enough so that if you try to read the A/D converter immediately after writing to base + 0, you will beat the A/D converter and get invalid data. Therefore the A/D converter provides a status signal to indicate whether it is busy or idle. This bit can be read back as bit 7 in the status register at Base + 8. When the A/D converter is busy (performing an A/D conversion), this bit is 1, and when the A/D converter is idle (conversion is done and data is available), this bit is 0. Here is a pseudocode explanation:

```
Status = read(base+8) AND 128 // or Status = read(base+8) AND 80 Hex
If Status = 0 then conversion is complete, else A/D converter is busy
```

Keep repeating this procedure until Status = 0.

8.6 Read the data from the board

Once the conversion is complete, you can read the data back from the A/D converter. The data is 16 bits wide and is read back in two 8-bit bytes. The following pseudocode illustrates how to construct the 16-bit A/D value from these two bytes:

```
LSB = read(base)
MSB = read(base+1)
Data = MSB * 256 + LSB        // combine the 2 bytes into a 16-bit value
```

The final data is interpreted as a signed value ranging from –32768 to +32767.

⇒ **Note:** The data range always includes both positive and negative values, even if the board is set to a unipolar input range. The data must now be converted to volts or other engineering units by using a conversion formula as shown on the next page.

Convert the numerical data to a meaningful value

Once you have the A/D value, you need to convert it to a meaningful value. The first step is to convert it back to the actual measured voltage. Afterwards you may need to convert the voltage to some other engineering units (for example, the voltage may come from a temperature sensor, and then you would need to convert the voltage to the corresponding temperature according to the temperature sensor's characteristics).

Since there are a large number of possible input devices, this secondary step is not included here; only conversion to input voltage is described. However you can combine both transformations into a single formula if desired.

To convert the A/D value to the corresponding input voltage, use the following formulas:

Conversion Formula for Bipolar Input Ranges

Input voltage = A/D value / 32768 * Full-scale input range

Example: Input range is ±5V and A/D value is 17761:
Input voltage = 17761 / 32768 * 5V = 2.710V

For a bipolar input range, 1 LSB = 1/32768 * Full-scale voltage.

Here is an illustration of the relationship between A/D code and input voltage for a bipolar input range (V_{FS} = Full scale input voltage):

A/D Code	Input voltage symbolic formula	Input voltage for ±5V range
-32768	$-V_{FS}$	-5.0000V
-32767	$-V_{FS}$ + 1 LSB	-4.9998V
…	…	…
-1	-1 LSB	-0.00015V
0	0	0.0000V
1	+1 LSB	0.00015V
…	…	…
32767	V_{FS} - 1 LSB	4.9998V

Conversion Formula for Unipolar Input Ranges

Input voltage = (A/D value + 32768) / 65536 * Full-scale input range

Example: Input range is 0-5V and A/D value is 17761:
Input voltage = (17761 + 32768) / 65536 * 5V = 3.855V

For a unipolar input range, 1 LSB = 1/65536 * Full-scale voltage.

Here is an illustration of the relationship between A/D code and input voltage for a unipolar input range (V_{FS} = Full scale input voltage):

A/D Code	Input voltage symbolic formula	Input voltage for 0-5V range
-32768	0V	0.0000V
-32767	1 LSB (V_{FS} / 65536)	0.000076V
…	…	…
-1	V_{FS} / 2 - 1 LSB	2.4999V
0	V_{FS} / 2	2.5000V
1	V_{FS} / 2 + 1 LSB	2.5001V
…	…	…
32767	V_{FS} - 1 LSB	4.9999V

9. A/D SCAN, INTERRUPT, AND FIFO OPERATION

The three control bits FIFOEN (FIFO enable), SCANEN (scan enable), and AINTE (A/D interrupt enable) determine the behavior of the board during A/D conversions.

In all cases, at the end of an AD conversion A/D data is latched into the FIFO in an interleaved fashion, first LSB, then MSB. A/D Data is read out of the FIFO with 2 read operations, first Base + 0 (LSB) and then Base + 1 (MSB).

When SCANEN = 1, each time an A/D trigger occurs, the board will perform an A/D conversion on all channels in the channel range. When SCANEN = 0, each time an A/D trigger occurs, the board will perform a single A/D conversion and then advance to the next channel and wait for the next trigger.

During interrupt operation, if FIFOEN = 1, then the FIFO will fill up with data until it reaches or exceeds half-full (half-full = 256 samples), and then the interrupt request will occur.

For all cases here where AINTE = 1, it is assumed that CLKEN = 1 as well, since in most applications interrupt operation is based on a hardware A/D clock.

AINTE	FIFOEN	SCANEN	Operation
0	0	0	Single A/D conversions are triggered by write to B+0. STS stays high during the A/D conversion. No interrupt occurs. The user program monitors STS and reads A/D data when it goes low.
0	0	1	A/D scans are triggered by write to B+0. All channels between LOW and HIGH will be sampled. STS stays high during the entire scan (multiple A/D conversions). No interrupt occurs. The user program monitors STS and reads all A/D values when it goes low.
0	1	0	Same operation as case 000 above.
0	1	1	Same operation as case 001 above.
1	0	0	Single A/D conversions are triggered by the source selected with CLKSEL. STS stays high during the A/D conversion. A/D interrupt occurs after each conversion is done (when STS goes low). The interrupt routine reads one A/D sample each time it runs.
1	0	1	A/D scans are triggered by the source selected with CLKSEL. STS stays high during the entire scan (multiple A/D conversions). A/D interrupt occurs after the entire scan is complete. The interrupt routine reads out one entire A/D scan (multiple values) each time it runs.
1	1	0	Single A/D conversions are triggered by the source selected with CLKSEL. STS stays high during the A/D conversion. A/D interrupt occurs when HF goes high (256 A/D conversions have occurred). The interrupt routine reads out 256 samples (half the FIFO) each time it runs.
1	1	1	A/D scans are triggered by the source selected with CLKSEL. STS stays high during the entire scan (multiple A/D conversions). A/D interrupt occurs after the scan is complete AND HF is high (i.e. an integral no. of scans has occurred and the FIFO is half full or more). The interrupt routine reads out enough complete scans to equal 256 or more samples each time it runs.

10. ANALOG OUTPUT CIRCUIT DESCRIPTION

10.1 Description

DMM-16R-AT uses a 4-channel 12-bit D/A converter (DAC) to provide 4 optional analog outputs. Model DMM-16-NA-AT does not include the analog outputs.

A 12-bit DAC can generate output voltages with the precision of a 12-bit binary number. The maximum value of a 12-bit binary number is 2^{12} - 1, or 4095, so the full range of numerical values that you can write to the analog outputs on Diamond-MM-16R-AT is 0 - 4095. The value 0 always corresponds to the lowest voltage in the output range, and the value 4095 always corresponds to the highest voltage.

⇒ **Note:** In this manual, the terms analog output, D/A, and DAC are all used interchangeably to mean the same thing.

10.2 Analog Output Wiring

All analog output signals should use one of the analog ground pins on the I/O connector (Agnd) as their common reference. Connecting the – input of the analog signal to digital ground will induce significant noise in the measurement and lower the measurement accuracy to approximately 8-10 bits. For lowest noise, use shielded wiring when possible, keep the wiring as short as possible, and avoid running analog signals in parallel with noisy power and digital signals or directly over noisy power and digital circuits. Sharing one Agnd pin among several analog outputs is acceptable and will not degrade measurements.

10.3 Resolution

The *resolution* is the smallest possible change in output voltage. For a 12-bit DAC the resolution is $1/(2^{12})$, or 1/4096, of the full-scale output range. This smallest change results from an increase or decrease of 1 in the D/A code, and so this change is referred to as 1 LSB, or 1 least significant bit. The value of this LSB is calculated as follows:

1 LSB = Output voltage range / 4096

Example: Output range = 0-5V;

Output voltage range = 5V – 0V = 5V

1 LSB = 5V / 4096 = 1.22mV

Example: Output range = ±5V;

Output voltage range = 5V – -5V = 10V

1 LSB = 10V / 4096 = 2.44mV

10.4 Output Range Selection

Jumper block J5 is used to select the D/A output range. Two selections need to be made.

First select whether you want fixed 5V or programmable D/A reference. For a fixed 5V reference install a jumper in location 5, and for programmable install a jumper in P. Do not install a jumper in both 5 and P simultaneously or unpredictable behavior will occur.

If you select programmable reference, the reference must then be programmed and calibrated using the Universal Driver software. After the reference has been programmed and calibrated one time, it will be stored in an EEPROM on the board and will be automatically recalled each time the board is powered up.

Next select bipolar or unipolar output. For bipolar output the outputs will swing between ± the selected reference, and for unipolar output the output will swing from 0V to the selected reference. For bipolar output install a jumper in the B position, and for unipolar output install a jumper in the U position. Again, do not install a jumper in both B and U simultaneously or unpredictable behavior will occur.

10.5 D/A Conversion Formulas and Tables

The formulas below explain how to convert between D/A codes and output voltages.

Conversion Formulas for Unipolar Output Ranges

Output voltage = (D/A code / 4096) * Reference voltage

D/A code = (Output voltage / Reference voltage) * 4096

Example: Reference voltage = 5V
Output range in unipolar mode = 0 – 5V
Full-scale range = 5V – 0V = 5V
Desired output voltage = 1V; D/A code = 1V / 5V * 4096 = 819.2 => 819

For a unipolar output range, 1 LSB = 1/4096 * Full-scale range, or 1.22mV in this example.

Here is an illustration of the relationship between D/A code and output voltage for a unipolar output range (V_{REF} = Reference voltage):

D/A Code	Output voltage symbolic formula	Output voltage for 0 – 5V range
0	0V	0.0000V
1	1 LSB (V_{REF} / 4096)	0.0012V
…	…	…
2047	V_{REF} / 2 - 1 LSB	2.4988V
2048	V_{REF} / 2	2.5000V
2049	V_{REF} / 2 + 1 LSB	2.5012V
…	…	…
4095	V_{REF} - 1 LSB	4.9988V

Conversion Formulas for Bipolar Output Ranges

Output voltage = ((D/A code – 2048) / 2048) * Output reference

D/A code = (Output voltage / Output reference) * 2048 + 2048

Example: Reference voltage = 5V
Output range in bipolar mode = ±5V
Full-scale range = 5V – (-5V) = 10V
Desired output voltage = 1V; D/A code = 1V / 5V * 2048 + 2048 = 2457.6 => 2458

For a bipolar output range, 1 LSB = 1/4096 * Full-scale range, or 2.44mV in this example.

Here is an illustration of the relationship between D/A code and output voltage for a bipolar output range (V_{REF} = Reference voltage):

D/A Code	Output voltage symbolic formula	Output voltage for ±5V range
0	-V_{REF}	-5.0000V
1	-V_{REF} + 1 LSB	-4.9976V
…	…	…
2047	-1 LSB	-0.0024V
2048	0	0.0000V
2049	+1 LSB	0.0024V
…	…	…
4095	V_{REF} - 1 LSB	4.9976V

11. GENERATING AN ANALOG OUTPUT

This chapter describes the steps involved in generating an analog output (also called performing a D/A conversion) on a selected output channel using direct programming (not with the driver software).

There are three steps involved in performing a D/A conversion:

1. **Compute the D/A code for the desired output voltage**
2. **Write the value to the selected output channel**
3. **Update the D/A**

11.1 Compute the D/A code for the desired output voltage

Use the formulas on the preceding page to compute the D/A code required to generate the desired voltage.

⇒ **Note:** The DAC cannot generate the actual full-scale reference voltage; to do so would require an output code of 4096, which is not possible with a 12-bit number. The maximum output value is 4095. Therefore the maximum possible output voltage is 1 LSB less than the full-scale reference voltage.

11.2 Write the value to the selected output channel

The four DACs share a single address for the LSB, Base + 1. Each DAC then has its own MSB address. Writing to the DAC's MSB address causes the 12-bit value to be loaded into the DAC. Therefore the LSB must be written first.

First use the following formulas to compute the LSB and MSB values:

LSB = D/A Code AND 255 ;keep only the low 8 bits

MSB = int(D/A code / 256) ;strip off low 8 bits, keep 4 high bits

Example: Output code = 1776

LSB = 1776 AND 255 = 240 (F0 Hex); MSB = int(1776 / 256) = int(6.9375) = 6

(In other words, 1776 = 6 * 256 + 240)

Now write these values to the selected channel:

Write LSB to Base + 1

Write MSB to Base + 4 , Base + 5, Base + 6, or Base + 7 depending on the channel no.

11.3 Update the D/A

Read from any address in the range Base + 4 through Base + 7 to update the DACs. All four DACs are updated at the same time, so you can write data to multiple DACs and then perform a single read operation from any of the four addresses to update all of them at once.

Any DAC that has not had new data loaded into it will maintain its current value.

12. AUTOCALIBRATION OPERATION

DMM-16R-AT includes a sophisticated auto calibration circuit that manages the calibration of both the A/D and the D/A circuitry. Operation is as follows.

12.1 Reference Voltages

The board contains a precision reference voltage chip that is selected for high stability over time and temperature. The value of the voltage output from this chip is measured at the factory. The board also contains some precision resistor divider ladders that produce intermediate voltages derived from the original reference. All these voltages are measured at the factory and their values are stored in an EEPROM on the board.

12.2 A/D calibration

When the A/D is calibrated, it measures these voltages using an extra input multiplexor reserved for calibration. The calibration software compares the measurements to the stored values and makes adjustments to the board to bring the measurements into tolerance (less than 2 LSBs max, in most cases less than 1 LSB). The adjustments are produced by controlling 4 8-bit DACs that are inserted at various points in the circuit. The DAC data is then stored in the EEPROM. Each of the valid A/D input ranges has its own set of calibration values, since each input range has slight offset and gain differences compared to each other range.

12.3 D/A Calibration

When the D/A is calibrated, the board performs a similar operation. The output of DAC 0 is routed through the calibration multiplexor. The offsets of the other three DACs relative to DAC 0 are measured at the factory and stored in the EEPROM. During calibration the average offset is added to the measured output of DAC 0, and this value is used as the comparison value to minimize overall errors. During D/A calibration the board can automatically determine the jumper configuration of the DACs based on their response to various output codes.

If the board is configured for programmable output range, the calibration software will first set and calibrate the output range, then calibrate the D/A.

12.4 Universal Driver Software Support

Calibration is simple when using the Diamond Systems Universal Driver software. Several functions are provided to manage the entire operation, and a demo program is included. For application developers targeting an operating system not supported by Universal Driver, the source code is included so you can incorporate it into your own program.

With the Universal Driver software, you have the option of recalling calibration values each time you change the input range, or leaving the current ones in place. Leaving the current ones in place will match the performance of other A/D boards which also use only a single set of calibration values. Recalling the values specific to the new input range will improve performance by a few LSBs but will result in a time delay since the data must be recalled from the EEPROM and loaded into the DACs.

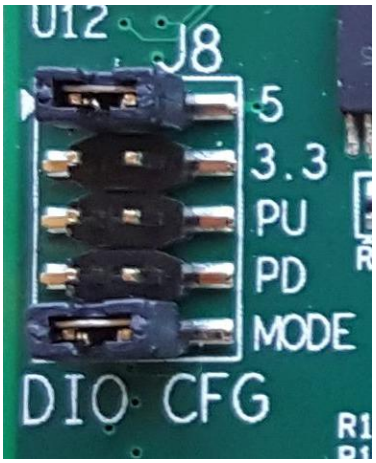
A/D and D/A maybe calibrated separately. Calibration takes a few seconds and may be performed as often as desired, for example at system startup, once a day, etc.

NOTE: When calibrating the D/A channels, the output voltage of DAC0 will fluctuate between – full scale and + full-scale as part of the procedure. Any circuitry connected to the DAC during this time may be affected and produce unwanted results.

13. DIGITAL I/O OPERATION

DMM-16R-AT contains two 8-bit digital I/O ports accessed on the I/O connector J3. The direction of both ports is programmable. Both ports will power up and reset with their output registers set to 0. For backwards compatibility with DMM-16-AT, on power up or reset the board configures port A for input and port B for output. Thereafter the port directions may be changed as desired.

When the ISA bus is used for the host interface, there are two available methods of accessing the DIO ports, Legacy and Enhanced mode. Selection is made with a jumper on jumper block J8. When the PCI bus is used, the DIO ports are always in Enhanced mode.



To facilitate full backward compatability with DMM-16-AT, selecting the Legacy mode (shown above) is required.

J8 Jumper description

Jumper on Pins 1&2	DIO 5V logic level
Jumper on Pins 3&4	DIO 3.3V logic level
Jumper on Pins 5&6	10K pull up for DIO
Jumper on Pins 7&8	10K pull down for DIO
Jumper on Pins 9&10	DIO Legacy mode
no Jumper on Pins 9&10	DIO Enhanced mode

In Legacy mode, the DIO ports are accessed at Base + 3. To access port B outputs, simply write an 8-bit value to base + 3. Similarly, to read the port A inputs, read from Base + 3.

In Enhanced mode, the port direction controls and registers and data are accessed in page 2. To select page 2, write 0x60 to base + 8.

Once page 2 is selected, register 12 is used to read/write port A, and register 13 is used to read/write port B (decimal addresses). The direction for each register is set with register 15. See the register map details earlier in this manual for complete details.

DIO port A bit 2 doubles as the gate control for Counter 0. When it is high, Counter 0 can count, and when it is low, Counter 0 holds its present value. If counter 0 is being used, make sure that this bit is set for the desired logic level. If the bit will be controlled externally, port A must be configured for input mode.

DIO port A bit 0 doubles as a programmable gate control for the 32-bit counter/timer. Bit 0 of the counter/timer control register at base + 10 determines whether this counter runs freely or whether DIO A0 is the gate. If the gate function is being used and is being provided externally, port A must be configured for input mode.

The digital I/O ports have two additional jumper configurations, logic level and pull resistor level. Logic level can be selected for either 3.3V or 5V. All DIO lines and the counter 0 external clock input are configured for the same voltage level. The input thresholds and output voltage levels for each nominal setting are listed in the specifications at the end of this manual.

The pull resistors can be configured for either up (3..3V or 5V depending on the logic level selection above) or down (ground). All DIO lines and the counter 0 external clock input are configured for the same direction. Note that this setting also affects the default value for DIO A2 (counter 0 gate) and DIO A0 (counter 1/2 gate) when these pins are not connected externally.

14. USER LED OPERATION

DMM-16R-AT provides a blue LED that is user programmable. This LED is typically used to verify that the board is properly configured and responding to software control. The board powers up and resets with the LED turned on.

The LED is accessed in page 2, register 14, bit 6. This is the only function of this register, so other bits may be ignored and overwritten without concern.

To select page 2, write 0x60 to base + 8.

To turn on the LED, write a 1 to bit 6 (write 0x40 to base + 14).

To turn off the LED, write a 0 to bit 6 (write 0x00 to base + 14).

15. COUNTER/TIMER OPERATION

DMM-16R-AT's FPGA contains an 82C54 counter/timer core that provides various timing functions on the board. The 82C54 core is configured as one 16-bit counter corresponding to counter 0 and one 32-bit counter/timer corresponding to counters 1 and 2 cascaded together. Counter 1's output is tied to counter 2's input, making counter 1 the lower 16 bits and counter 2 the upper 16 bits of the resulting 32-bit counter.

All 82C54 counting modes are supported; refer to any 82C54 datasheet for more information. Most applications on the DMM-16R-AT will use the counters in one of the following modes:

- Repetitive rate generator mode for A/D sampling
- Repetitive rate generator for counter 0 driven bus interrupts
- One-shot mode to count input pulses on counter 0

The counters operate in down counting direction only and can generate an output pulse upon reaching a count of 0. The count register is loaded with the desired frequency divider value and decrements by 1 each time a clock edge appears at the input. The number of input clocks can be determined by reading the current count register and subtracting it from the original value.

On DMM-16R-AT counter 0 is made fully available to the user. The input is on pin 29 of the I/O connector (IN0-). A rising edge on the input will cause the counter to decrement. The gate is on pin 46 of the I/O connector (DIO A2 / GATE0). When this pin is high, Counter 0 is enabled and can count. When this pin is low, Counter 0 holds its current value and ignores input clocks. Counter 0's output is on pin 31 (OUT0).

The 32-bit counter/timer is used to control the A/D sampling rate. The input to the counter is a fixed 10MHz clock provided by the board. The gate signal is available on pin 48 (DIO A0 / Gate 1/2).

Pin 29 (IN0-) and all the digital I/O lines (pins 33-48) on the I/O connector are connected to 10KΩ pull resistors to hold them in a steady state if unconnected. The pull-up/down setting is controlled with jumper block J8. If the resistors are configured for pull-down then a valid logic 1 needs to be applied to DIO A2 / Gate 0 for counter 0 to run, and a logic 1 needs to be applied to DIO A0 / Gate 1/2 for the 32-bit counter to run.

16. SPECIFICATIONS

Analog Inputs

No. of inputs	8 differential or 16 single-ended (user selectable)
A/D resolution	16 bits (1/65,536 of full scale)
Input ranges	Bipolar: ±10V, ±5V, ±2.5V, ±1.25V Unipolar: 0-10V, 0-5V, 0-2.5V
Input bias current	50nA max
Maximum input voltage	±10V for linear operation
Overvoltage protection	±35V on any analog input without damage
Nonlinearity	±3LSB, no missing codes
Conversion rate	100,000 samples per second max
Conversion trigger	software trigger, internal pacer clock, or external logic signal

Auto calibration

Circuits calibrated	A/D (all 8 input ranges) and D/A (fixed and programmable ranges)
A/D error	±1LSB (typical), ±2LSB (max) after autocalibration
D/A error	±1LSB (typical), ±2LSB (max) after autocalibration

Analog Outputs

No. of outputs	4
D/A resolution	12 bits (1/4096 of full scale)
Output ranges	Unipolar: 0 – 5V or 0 – (user-programmable) Bipolar: ±5V or ± (user-programmable)
Output current	±5mA max per channel
Settling time	4μS max to ±1/2 LSB
Relative accuracy	±1 LSB
Nonlinearity	±1 LSB, monotonic
Reference Voltage	5.000V ±3mV; 5mA max output current

Digital I/O

No. of IOs	16, HCT/TTL compatible (3.3V/5V jumper configurable)
Input voltage	5V operation: Logic 0: 0.0V min, 1.65V max; Logic 1: 3.35V min, 5.0V max 3.3V operation: Logic 0: 0.0V min, 0.8V max; Logic 1: 2.0V min, 3.3V max
Input current	±1μA max
Output voltage	5V operation: Logic 0: 0.0V min, 0.44V max; Logic 1: 3.76V min, 5.0V max 3.3V operation: Logic 0: 0.0V min, 0.44V max; Logic 1: 2.25V min, 3.3V max
Output current	Logic 0: 24mA max; Logic 1: -24mA max (both 5V and 3.3V operation)
Pull resistors	10K ohms +/-1% jumper-selectable for up or down, all ports same direction

Counter/Timers

A/D Pacer clock	32-bit down counter (2 82C54 counters cascaded)
Pacer clock source	10MHz or 1MHz on-board clock source
General purpose	16-bit down counter (1 82C54 ctr); 100KHz or external input

General

Bus interface	PC/104 bus: 8 bits, 5V; PCI-104 bus: 8 bits, 3.3V
Power supply	+5VDC ±5%
Current consumption	DMM-16R-AT: 390mA typical; DMM-16RP-AT: 375mA typical
±15V output current	±10mA max with DACs unloaded; **not short-circuit protected**
+5V output current	Limited by PC/104 power supply; **not short-circuit protected**
Operating temperature	-40 to +85°C
Operating humidity	5% to 95% noncondensing
Weight	DMM-16R-AT: 64g / 2.25oz; DMM-16RP-AT: 80g / 2.84oz